IN THE U[illegible]ED STATES PATENT AND TRADEMAR[illegible]FFICE

PATENT APPLICATION

Group Art Unit 2827 cp 28275

Examiner: I. PATEL

Inventor(s): HIROSE et al.

Appln. No.: 09 (Series Code ↑) 787,321 (Serial No. ↑)

Atty. Dkt. P 276725 (M#) 7031PU (Client Ref)

Filed: March 16, 2001

Appln. Title: MULTI-LAYER BUILD-UP WIRING BOARD

Hon. Commissioner of Patents
Washington, D.C. 20231

OIPE JC:188 JUL 15 2002 PATENT & TRADEMARK OFFICE

Sir:

REPLY/AMENDMENT/LETTER

Date: July 15, 2002

This is a reply/amendment/letter in the above-identified application and includes the herewith attachment of same date and subject which is incorporated hereinto by reference and the signature below is treated as the signature to the attachment in absence of a signature thereto.

FEE REQUIREMENTS FOR CLAIMS AS AMENDED

1. Small Entity claim
A. ☒ NOT made
B. ☐ Withdrawn
C. ☐ made herewith
D. ☐ made previously
For B & C See Required Separate Paper (Pat-256)

	Claims remaining after amendment	Highest number previously paid for		Present Extra	Large/Small Entity	Additional Fee	Fee Code Lg/Sm
2. Total Effective Claims	17	**minus	20	0	x $18/$9 =	+ $0	103/203
3. Independent Claims	3	***minus	13	0	x $84/$42 =	+ $0	102/202
4. If amendment enters proper multiple dependent claim(s) into this application for first time (leave blank if this is a reissue application) ..... add					+ $280/$140 =	+ $0	104/204
5. Original due Date: June 14, 2002	☐ NONE						
6. Petition is hereby made to extend the original due date to cover the date this response is filed for which the requisite fee is attached		(1 mo) (2 mos) (3 mos) (4 mos) (5 mos)		$110/$55 = $400/$200 = $920/$460 = $1,440/$720= $1,960/$980=	+ $110		115/215 116/216 117/217 118/218 128/228
7. Enter any previous extension fee paid since above original due date and subtract					- $0		
8.					Extension Fee	+ $110	
9. If Terminal Disclaimer attached, add Rule 20(d) official fee					+ $110/$55	+ $0	148/248
10. If IDS attached requires Official Fee under Rule 97 (c), ... add or if Rule 97(d) Request ..... add					+ $180 + $180	+ $0	126 126
11. After-Final Request Fee per rules 129(a) and 17(r)					+ $740/370	+ $0	146/246
12. No. of additional inventions for examination per Rule 129(b).....					x $740/370 ea	+ $0	149/249
13. Request for Continued Examination (RCE)					+ $740/370	+ $0	1179/1279
14. Petition fee for						+ $0	
15.					TOTAL FEE =	$110	

16. *If the entry in this space is less than entry in next space, the "Present Extra" result is "0".
17. **If the "Highest number previously paid for" in this space is less than 20, write "20" in this space.
18. ***If the "Highest number previously paid for" in this space is less than 3, write "3" in this space.

PLEASE CHARGE OUR DEP. ACCT

Our Deposit Account No. 03-3975)
(Our Order No. 41226 (C#) 276725 (M#)

CHARGE STATEMENT: The Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fee(s) filed, or asserted to be filed, or which should have been filed herewith or concerning any paper filed hereafter, and which may be required under Rules 16-18 (missing or insufficiencies only) now or hereafter relative to this application and the resulting Official Document under Rule 20, or credit any overpayment, to our Accounting/Order Nos. shown above, for which purpose a duplicate copy of this sheet is attached.
This CHARGE STATEMENT does not authorize charge of the issue fee until/unless an issue fee transmittal sheet is filed.

Query: Is appeal deadline now? If so, file Notice of Appeals separately.

Pillsbury Winthrop LLP
Intellectual Property Group
By Atty: Glenn J. Perry Reg. No. 28458
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Atty/Sec: GJP/TPT/smm

NOTE: File this cover sheet in duplicate with PTO receipt (PAT-103A) and attachments

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION OF
HIROSE et al.
Appln. No.: 09/787,321
Filed: March 16, 2001
Title: MULTI-LAYER BUILD-UP WIRING BOARD

Confirmation No.: 7824
Group Art Unit: 2827
Examiner: I. PATEL

#12/C
Ext. 1 mo
J.M Cannon
7/25/02

July 15, 2002

* * * * *

AMENDMENT UNDER 37 C.F.R. § 1.111

Hon. Commissioner of Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated March 14, 2002, please amend the above identified application as follows:

IN THE SPECIFICATION:

Please delete the specification and replace it with the Substitute Specification submitted herewith.

IN THE CLAIMS:

Please cancel claims 1-14 without prejudice.

Please add the following new claims:

15. (New) A multilayer buildup-wiring board comprising:

a core substrate;

a plurality of conductor layers;

a plurality of insulating layers;

wherein said plurality of conductor layers and said plurality of insulating layers are alternately stacked on at least one side of said core substrate; and

wherein a plurality of mesh holes are formed in each of said conductor layers; and

wherein each of said plurality of mesh holes formed in each of said plurality of conductor layers is disposed so that at least part of each of said mesh holes overlays one of said plurality of mesh holes in each of the remaining conductor layers.

16. (New) A multilayer buildup-wiring board as in claim 15,

wherein a plurality of mesh holes are formed in said core substrate; and

wherein each of said plurality of mesh holes formed in said core substrate is disposed so that at least part of each of said mesh holes overlays one of said plurality of mesh holes formed in each of said conductor layers.

17. (New) A multilayer buildup-wiring board as in claim 15,

wherein a diameter of each of said mesh holes is set at 75 to 300 μm; and

wherein a distance between said mesh holes is set at 100 to 1500 μm.

18. (New) A multilayer buildup-wiring board as in claim 15, further comprising:

a chip mount region disposed on a portion of the outermost layer; and

a plurality of via holes or through holes with lands disposed in at least a portion of said mesh holes in a region facing said chip mount region through said insulating layers;

wherein said conductor layers are electrically connected to each other through said via holes; and

wherein a plurality of conductor pads connected to lands of at least a portion of said via holes or through holes.

cont'd C1

19. (New) A multilayer buildup-wiring board as in claim 15, further comprising:

a chip mount region disposed on a portion of the outermost layer; and

a plurality of via holes with lands disposed in at least a portion of said mesh holes in a region facing said chip mount region through said insulating layers; wherein

said conductor layers are electrically connected to each other through said via holes.

20. (New) A multilayer buildup-wiring board as in claim 15, further comprising:

a chip mount region; and

solid conductor layers disposed in at least a portion of the mesh holes in a region facing said chip mount region through said insulating layers.

21. (New) A multilayer buildup-wiring board as in claim 15, further comprising:

a chip mount region disposed on a portion of the outermost layer; and

a plurality of through holes with lands disposed in at least a portion of said mesh holes in a region facing said chip mount region through said insulating layers; wherein

said conductor layers are electrically connected to each other through said through holes.

22. (New) A multilayer buildup-wiring board as in claim 18,

wherein a plurality of electrical wiring paths are provided in at least one of said plurality of via holes formed in said mesh holes; and

wherein each of said plurality of electrical wiring paths is not electrically connected to any other electrical wiring path disposed in said via hole.

23. (New) A multilayer buildup-wiring board as in claim 22,

wherein two electrical wiring paths are disposed in at least one of said plurality of via holes formed in said mesh holes.

cont'd Cl

24. (New) A multilayer buildup-wiring board as in claim 16, comprising:

a plurality of electrical wiring paths provided in each of the through holes in said core substrate;

wherein each of said plurality of electrical wiring paths is not electrically connected to any other electrical wiring path disposed in said mesh hole.

25. (New) A multilayer buildup-wiring board as in claim 24, wherein conductor layers are disposed on both sides of said core substrate; and

wherein conductor layers on opposite sides of the core substrate are electrically connected by through holes in said core substrate.

26. (New) A multilayer buildup-wiring board as in claim 24, wherein each of said plurality of through holes formed in said core substrate is filled with a filler;

wherein a conductor layer covers the exposed surface of said filler;

wherein each of said conductor layers is divided into a plurality of parts; and

wherein said electrical wiring paths formed in said through holes of said core substrate are electrically connected to said plurality of parts of said conductor layers.

27. (New) A wiring board comprising:

a conductor circuit including at least one conductor layer;

wherein said conductor layer is comprised of a two-layer structure in which a second metal film thinner than a first metal film is disposed on said first metal film; and

wherein the area covered by the second metal film forming said conductor layer is larger than the area covered by said first metal film, said films disposed so that the entire periphery of said first film is inside of the periphery of said second film.

28. (New) A multilayer buildup-wiring board comprising;

at least one resin insulating layer;

at least one conductor circuit;

wherein said conductor circuit includes at least one conductor layer;

Cont'd C1

wherein said conductor layer is comprised of a two-layer structure in which a second metal film thinner than a first metal film is disposed on said first metal film;

wherein the area covered by the second metal film forming said conductor layer is larger than the area covered by said first metal film; and

wherein said films are disposed so that the entire periphery of said first film is inside of the periphery of said second film.

29. (New) A multilayer buildup-wiring board as in claim 18, wherein said lands or conductive pads are formed with a distance kept between said lands or conductive pads and a peripheral edge of said mesh holes.

30. (New) A multilayer buildup-wiring board as in claim 19, wherein said lands or conductive pads are formed with a distance kept between said lands or conductive pads and a peripheral edge of said mesh holes.

31. (New) A multilayer buildup-wiring board as in claim 21, wherein said lands or conductive pads are formed with a distance kept between said lands or conductive pads and a peripheral edge of said mesh holes.

REMARKS

Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Claims 15-31 are pending in the application.

Claims 1-14 have been cancelled.

The drawings have been objected to for identifying figures with secondary reference numbers which are continuations from previous figures, and for failing to identify Fig. 9(C) and 23 as prior art. Applicants have made appropriate corrections to the drawings. Further, as the corrections made to the drawings have necessitated numerous corrections to the specification, Applicants are submitting a Substitute Specification with this Amendment.

Claims 1-7 have been rejected under 35 U.S.C. § 102(a) as being anticipated by Akira Wakasaki (JP10163634). Applicants respectfully traverse this rejection.

The rejection of claims 1-7 is moot, as claims 1-7 have been cancelled. Applicants, however, will address the rejection, as new claims added by this Amendment contain substantially the same features as cancelled claims 1-7.

The Examiner asserts that Akira discloses a multilayer build-up wiring board with mesh holes formed in a plurality of conductive layers so that at least part of the mesh holes overlay one another. This is incorrect. Referring to Fig. 1 of Akira, the mesh holes H of one conductive layer clearly do not overlay the mesh holes H of adjacent conductive layers. Each mesh hole of each conductive layer is disposed so as to be directly above/below a solid portion of adjacent conductive layers.

In contrast, the mesh holes formed in the conductive layers of the present invention, as claimed by claims 15-26 and 29-31, claim a multilayer build-up wiring board with mesh holes formed in a plurality of conductive layers so that at least part of the mesh holes overlay one another. This configuration helps to prevent deterioration of the electrically insulating properties of the insulating layers disposed between conductive layers (page 3, lines 4-5). Claims 15-26 and 29-31, therefore, contain features neither disclosed or suggested by Akira, and are in form for allowance.

Claims 8-12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Akira in view of Iadorola (USPN 4,543,715). Applicants respectfully traverse this rejection.

As for claims 1-7, the rejection of claims 8-12 is moot, as claims 8-12 have been cancelled. New claims 22-26, however, contain substantially the same features as cancelled claims 8-12, so the Examiner's rejection will be addressed.

As explained above, claims 22-26 claim the feature of a multilayer build-up wiring board with mesh holes formed in a plurality of conductive layers so that at least part of the mesh holes overlay one another, which is neither disclosed or suggested by Akira, Iadorola, or any combination of the two.

Further, claims 22-26 claim the feature of a plurality of electrical wiring paths provided in each of the through holes in said core substrate, wherein each of said plurality of electrical wiring paths is not electrically connected to any other electrical wiring path disposed in said mesh hole.

In contrast, Iadorola discloses split via holes with divided circuit lines which are electrically connected. Referring to Fig. 1 of Iadorola, it can be seen, for example, that circuit trace 23 electrically connects divided circuit lines going through a specific via hole. Iadorola, therefore, does not disclose or suggest the feature, as claimed by claims 22-26 of the present invention, of a plurality of electrical wiring paths in one via hole which are not electrically connected.

Claims 22-26, thus, are in form for allowance.

Claims 13-14 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Akira in view of Dinella et al. (USPN 4,081,601). Applicants respectfully traverse this rejection.

The rejection of claims 13-14 is moot, as claims 13-14 have been cancelled. Claims 27-28, however, contain substantially the same features as claims 13-14.

Akira does not disclose or suggest a wiring board with a conductive layer with a two-layer structure, let alone a two-layer structure with one layer having different dimensions than the other layer, configured so that the periphery of one layer protrudes beyond the periphery of the other layer at all points.

Dinella discloses multi-laminated conductive layers wherein each layer has the same length and width, configured so that the periphery of all layers coincide.

In contrast, claims 27-28 of the present invention claim a wiring board with a conductive layer, "wherein said conductor layer is comprised of a two-layer structure in which a second metal film thinner than a first metal film is disposed on the first metal film; and wherein the area covered by said second metal film forming said conductor layer is larger than the area covered by said first metal film, said films disposed so that the entire periphery of said first film is inside of the periphery of said second film." No combination of Dinella and Akira discloses or suggests such features.

Claims 27-28, therefore, are in form for allowance.

CONCLUSION

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

PILLSBURY WINTHROP LLP

By: _____

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